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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,954	03/22/2004	Vivien Wong	SC13116MP	2592

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EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,954	WONG ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-13, & 15-20* is/are rejected.

7)☒ Claim(s) *2 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 & 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boccali et al., US 4,319,193, in view of Koebke, US 5,028,873.

As per Claim 1, Boccali discloses a relay tracker circuit (FIG. 7) for counting clicks (ABS., lines 7-8) of a plurality of relays (column 4, lines 17-18), the relay tracker circuit comprising:

- a controller **42** including a counter **48** for counting relay clicks of the plurality of relays (column 9, lines 42-44);
- a plurality of wires (see FIG. 7) connecting the controller **42** to the relays (at test stations **60-63**), wherein each time a relay switches, a signal is transmitted from the relay to the controller and the controller increments a counter therefor; and
- a memory **41** connected to the counter **48** (via **75** to bus **80** to memory **41**) for storing the count information for each relay (column 9, lines 47-49).

Boccali does not disclose the relays on a load board.

Koebke discloses the use of the relays on a load board (ei. printed circuit board, column 1, lines 9-10).

Therefore, it would have been obvious to a person of ordinary skill in the art to use a load board, as taught by Koebke, in the relay tracking system of Boccali, in order test the relays in different modes of operation (column 2, line 59).

As per Claim 10, Boccali discloses that the plurality of wires comprise conductive traces (column 8, line 56).

As per Claim 11, as best understood by the examiner, based on the specification and drawings, the DUT's and the relays refer to the same component.

Boccali discloses an interface (68-71) for applying simulated loads from a test system to one or more devices under test (DUTS), comprising:

- a plurality of conductive traces (see FIG. 7, ei. connection between **68-71** and **60-63** respectively) for transmitting signals from the test system to the DUTS (relays at **60-63**);
- a plurality of relays (relays at stations **60-63**) connected to the plurality of traces for performing signal switching (**68-71**); and
- an embedded relay tracker circuit (**42** & **41**) connected to the plurality of relays for counting (counter in **48**) relay clicks and generating and storing (in **41**) relay usage information (column 9, lines 47-49).

Boccali does not disclose the use of a load board for applying the test loads.

Koebke discloses the use of a load board (ei. printed circuit board, column 1, lines 9-10) for applying test load to the relays.

Therefore, it would have been obvious to a person of ordinary skill in the art to use a load board for applying the simulated loads to the relays, as taught by Koebke, in the relay tracking system of Boccali, in order test the relays in different modes of operation (column 2, line 59).

As per Claim 12, Boccali further discloses the embedded relay tracker circuit includes an interface **75** for connecting the tracker circuit to a computer **41** and passing the relay usage information to the computer **41** for display (see FIG. 7, information is transmitted via **74** to **75** wherein the data is transmitted via **80** to **41**).

As per Claim 13, Boccali further discloses embedded relay tracker circuit including:

- a controller **42** including a counter (in **48**) for counting relay clicks (column 9, lines 42-44) of the plurality of relays (in **60-63**);
- a plurality of wires connecting the controller to the relays (see FIG. 7, ei. the traces between **42** and **60-63**), wherein each time a relay switches, a signal is transmitted from the relay to the controller and the controller increments a counter therefor (column 9, lines 42-44); and
- a memory **41** connected to the counter for storing the count information for each relay (column 9, lines 47-49).

3. Claims 3-9 & 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boccali et al. in view of Koebke, as applied to claims 1 & 13 above, and further in view of Reid et al., US 5,892,449.

As per Claims 3-6 & 15-17, Boccali et al. in view of Koebke disclose a relay tracker load board circuit as applied to Claims 1 & 13 above.

Boccali as modified does not explicitly disclose the memory **41** to comprise of RAM and EEPROM wherein the RAM and EEPROM are integral with the controller.

Reid discloses a load center for relays (column 3, lines 55-57), interpreted here as a relay tracker system wherein the memory comprises:

- RAM **57b** (FIG. 3)
- EEPROM **57c** (FIG. 3)
- Wherein the RAM and EEPROM are integral to the controller **32** (FIG. 3, column 4, lines 26-32).

Therefore it would have been obvious to a person of ordinary skill in the art to use RAM and EEPROM which are integral to the controller, as taught by Reid, in the system of Boccali as modified, in order to have a temporary memory storage using the RAM and an erasable memory storage using the EEPROM, wherein the RAM and EEPROM are integral in the controller for operator convenience and control (Reid: column 4, lines 22-23, 29-32).

As per Claims 7 & 18, Boccali et al. in view of Koebke and Reid disclose a relay tracker load board circuit as applied to Claims 6 & 17 above

Boccali as modified does not disclose the storing the count information in RAM while the load board is connected to a test head.

Reid discloses storing wherein the count information (column 9, lines 43-47) in the RAM 256 (FIG. 6, column 9, lines 24-25) while the load board is connected to a test head (ei. during operation, column 9, lines 43-47).

Therefore, it would have been obvious to a person of ordinary skill in the art to store count data in RAM, as taught by Reid, in the system of Boccali as modified, in order to have a temporary memory storage using the RAM (Reid: column 4, lines 29-32).

As per Claims 8 & 19, Boccali et al. in view of Koebke and Reid disclose a relay tracker load board circuit as applied to Claims 7 & 18 above

Boccali as modified does not disclose including a capacitor connected to the controller for providing power to the controller when the controller is disconnected from the test head and the power source.

Reid discloses a capacitor connected to the controller for providing power to the controller when the controller is disconnected from the test head and the power source (column 5, lines 20-25).

Therefore, it would have been obvious to a person of ordinary skill in the art to use a capacitor, as taught by Reid, in the system of Boccali as modified, for power supply storage (Reid: column 5, lines 20-25).

As per Claims 9 & 20, Boccali et al. in view of Koebke and Reid disclose a relay tracker load board circuit as applied to Claims 8 & 19 above.

Boccali as modified does not disclose moving the count information from the RAM to the EEPROM when the load board is disconnected from the test head.

Reid discloses storing the relay information in the RAM as long as possible and writing the information to the EEPROM at prescribed times (column 4, lines 42-43). Therefore it would be obvious to set the prescribed time to the time the test head is disconnected.

Therefore, it would have been obvious to a person of ordinary skill in the art to move the count information from the RAM to the EEPROM, as taught by Reid, in the system of Boccali as modified, in order to store data until it required to be erased (column 4, lines 31-32).

Allowable Subject Matter

4. Claims 2 & 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach of allocating about four bytes of space in the memory per relay.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ohgake et al., US 4,689,570, discloses a system for tracking relays including a controller and a counter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858

MK

ANJAN DEB
PRIMARY EXAMINER